# Testing the HP-65 Logic Board

*The board and its automatic test system are designed for rapid production testing and troubleshooting.*

**by Kenneth W. Peterson**

DESIGNING AN INSTRUMENT for minimum cost means not only that parts and assembly costs are minimized. The time required for testing, troubleshooting, and repair is also critical and must be held to an absolute minimum. Yet too many products are designed without giving adequate consideration to the time that can be spent analyzing and locating any faults that may show up in production testing.

For a high-volume, complex product like the HP-65, computerized testing is the only feasible method. To aid the computer in diagnosing failures and isolating them to the responsible components, it's essential that access be provided to all of the product's pertinent nodes. The HP-65 logic board was designed with this in mind.

The layout of the HP-65 logic board is shown in Fig. 1. Input and output lines are brought out to two edges of the board. Additional test points are routed to a third edge, giving access to a total of 45 test points.

### Test System

A block diagram of the computerized tester designed for the HP-65 logic board is shown in Fig. 2. The tester functionally compares the operation of a known-good unit with that of a test unit. All outputs from the test logic board are interfaced to voltage-comparison circuits to check for proper logic-level thresholds.

As the tester exercises the reference and test units with identical inputs (either on the key lines or on the card reader lines), the units' outputs are captured in two pattern storage registers on each clock time.

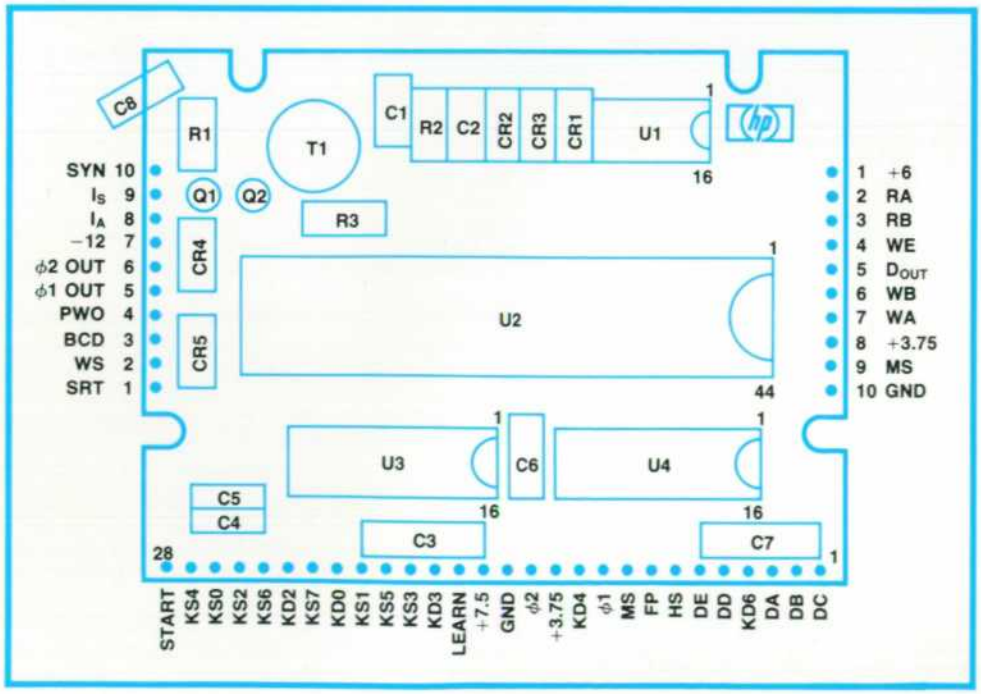


**Fig. 1.** *The HP-65 logic board is designed for automatic testing. Access to 45 test points is provided.*

The patterns are continually compared. If they ever fail to compare, their error condition is frozen in the pattern storage registers and a flag is sent to the computer. The computer can then request all pertinent information from the tester, which keeps a record of events leading up to a failure. For example, microinstructions are saved and decoded to show which chip was talking on the calculator buses when the failure occurred. Other information retained by the tester is the present ROM address, the previous ROM address, the identity of the active ROM (one of twelve), the bit count at the time of failure, and the number of word times since the start of the test sequence.

All this information and the contents of the two pattern storage registers are then sent to the computer. The computer sorts through the data with the aid of a diagnostic table and prints out the nature of the error and the component most likely to have caused it.

### Tester Architecture

The HP-65 logic board tester has six main parts.

The *controller* is a 32-state ROM machine with 16 qualifiers and two-way branching on test conditions. There are eighteen instruction lines. Each state issues instructions that control the condition of other hardware in the tester. The controller also contains the master clock, a crystal-controlled oscillator set to the specified limit of the MOS circuits, 200 kHz.

The *interface circuits* consist of a voltage comparator and buffer amplifier between each calculator's MOS circuits and the input to the pattern storage register, which is a TTL circuit. The voltage comparator checks the upper and lower limits of the logic levels.

The *pattern storage and comparator circuit* consists of two 16-bit registers of D-type flip-flops with a 16-bit parallel comparison circuit between them to check for parity. If the patterns do not compare after each clock period (5$\mu$s) an error flip-flop is set. The clock is then inhibited to each of the 16-bit pattern storage registers and the error condition is saved.

*Input/output* information is received by the tester and transmitted to the computer over 16 parallel lines. Inputs are stored in a 16-bit buffer register which receives commands and data from the computer. Three of the input lines from the computer are assigned as output select control lines to specify which data to send back to the computer. The other 13 input lines are used to control the logic board: six lines specify the key code (function), four lines simulate switches to the card reader, one line varies the power-supply limits, and two lines are used for status information.

A 16-bit, eight-channel multiplexer controlled by the three output-select lines is used to return data to the computer. A full handshake between the tester and the computer is done; this assures proper data-transmission timing.

*Inputs* to the logic board are either through the key lines or the card reader control lines. The key lines are made through an 8 × 5 matrix. A six-bit code

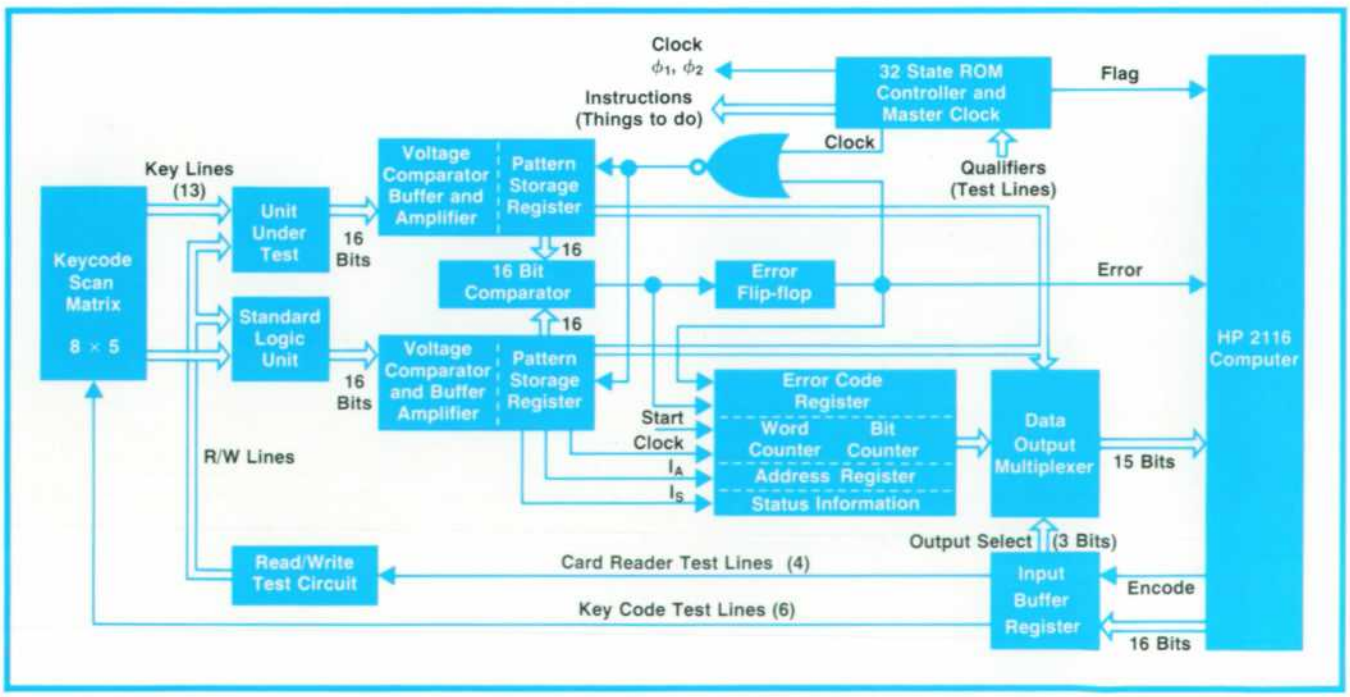


**Fig. 2.** *Logic board tester compares a reference board with a test board. Failures are analyzed by the computer, which prints out diagnostic messages.*

from the computer specifies the key code. There are four lines to the card reader: learn mode switch, motor switch, head switch, and file protect switch.

The *read/write test circuit* is a 15-state controller with instruction decoding for determining when to shift the read/write data pattern in and out. To simulate the magnetic card, reference write patterns are stored in two 600-bit shift registers. A third 600-bit shift register is used as a counter to keep track of how many shifts have been done.

### Card Reader Testing

To make the card reader circuit read or write it is necessary to close the motor switch and the head switch. Then the condition of the learn mode switch line specifies whether the unit will read or write. The file protect line specifies the condition of the write enable line.

The test sequence consists of writing a test pattern from each of the two logic boards and comparing the pattern of the reference board to that of the board under test. The reference patterns are stored in two 600-bit shift registers. The next step is to read the same pattern back into the calculator and then write it back out again. The second write sequence is used to verify that the read circuit is functioning properly. The write enable line is tested by making the file protect signal a logical zero on the first write sequence and a logical one during the second write sequence.

### Overall Test Sequence

The steps in the test sequence are as follows:

- Power off, push start button.
- Turn power on, set time delay (this allows the power supply to rise to the proper level).
- Test power supply and clock for proper high and low limits. Also test if power-on pulse was given properly. If not go to error routine.
- If everything is correct give a pseudo power-on (PWO) signal. This sets the starting address to zero.
- Test if both systems are in synchronism and if not, slow the clock to the unit under test until both systems are in synchronism.
- Release power-on pulse and start comparison test. When display has turned on and no error has occurred, flag computer for first key code sequence.
- After receiving first key code, enable key code matrix and continue to enable until display turns off.
- Wait until calculator display has turned back on again.
- Test if calculator is ready for its next test sequence, which can be through the key lines again or through the card reader lines.
- The test sequences are continued until the computer gives an end code. Then the "good" light turns on.
- If an error occurs the tester generates an error code corresponding to that fault. The computer is then flagged with the error line high.
- The computer then sends back a series of output select codes to specify which information is to be sent back to the computer. After the computer has received all information from the tester, an end code is sent to the tester. The tester turns on a "bad" light.
- The computer then prints out diagnostic messages.

### Test Time

The time required for testing a logic board is determined by the number of test sequences and the length of time of each function. Typical test time is about one minute for the complete test sequence, that is, for a good board.


### Acknowledgments

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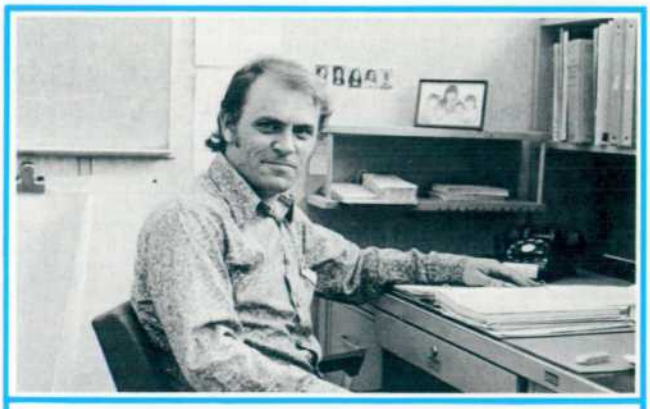

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Ken Peterson, a member of HP Laboratories since 1965, has worked on the 2116 Computer, the 9100 Calculator, and all of HP's pocket calculators. Ken was a radar technician in the U.S. Air Force and later studied electronics for two years at a community college. His home is in Fremont, California, just south of his native Oakland, and he frequently attends Oakland Raiders' professional football games, especially enjoying it when the Raiders beat their rivals, the Kansas City Chiefs. He's a softball player and a skier, too. He and his wife Carmen have five daughters ranging in age from four months to fourteen years.